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10/055,992	01/28/2002	Norifumi Kobayashi	02887.0213	2127

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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,992	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 were rejected in Office Action of 27 July 2005. Applicants' response of 27 December 2005 has amended claims 1-21 and presented new claims 22-27.

Claims 1-27 have been rejected.

Specification

The previous objections to the specification have been withdrawn in light of the amendments thereto.

Claim Objections

1. Claims 1-27 are objected to because of the following informalities: The numerous amendments to the claim language make it difficult to understand what Applicants are claiming. The claims appear to be a translation from a foreign language and in numerous instances the accuracy of the translation is suspect.

In claims 1-27, in response to the previous objection to the term "dispersion" in the claims, Applicants submit that "variation" and "dispersion" are synonymous and have replaced every occurrence of the word "dispersion" with the term "variation." It is unclear how this change affects the claim scope, or alternatively how this amendment could possibly overcome the ambiguity present in the term "dispersion." It is noted that "dispersion and variation are interchangeable in the context of the present invention" (Applicants' response, page 12).

Indeed, Applicants' response states for the record that "[The term] 'variation' is not used explicitly in the specification" (Applicants' response, page 12). It appears that this amendment is intended only to perpetuate the unconventional terminology used in the claims. It is unknown whether Applicants use of this term constitutes new matter because it remains unknown what is a proper and precise definition for both "dispersion" and "variation" in the context of the claims.

2. Claim 1 recites several instances of functional language that do not further limit the claim. Although not improper under 35 U.S.C. § 112, Applicants have submitted arguments regarding these limitations as though they are required. The Examiner respectfully draws Applicants attention to language such as "said delay information operating part further receiving design information of the integrated circuit to prepare a delay information file incorporating each influence of said variation for each location in the chip on the basis of said variation rule file and said design information," which in the context of an apparatus-style system claim, does not further limit the invention. This language recites a step of receiving and an intent to prepare a delay information file but does not recite a step of preparing.

3. Claims 2, 9, and 16 recite "said delay information file includes the modified design information," or a similar limitation, which does not appear to reflect the invention as described in claim 1. In claim 1, it appears that the "delay information file incorporates each influence of said variation for each location in the chip on the basis of [both] said variation rule file and said design information." This language does not clearly state that the delay information file includes

design information. If it is Applicants' intent that the "delay information file" explicitly includes "said design information" in claim 1, clarification is respectfully requested.

4. Claims 3, 10, and 17 recite "an information classifying unit which classifies said information on said variation into groups of an arbitrary size, the chip including said groups," or a similar limitation, which appears to be incorrect English. The claim language literally recites that the chip includes arbitrary sized groups of information (in contrast to circuit components). Presumably, as is known in the art, the chip itself is divided into "groups of an arbitrary size," often referred to as cells, and the "information on variation" is divided to correspond to those cells. Of course, the claim does not reflect this.

Applicants are also advised that "groups of arbitrary size" would be the epitome of a relative term and indefinite under 35 U.S.C. § 112, second paragraph, in the event that such a limitation were relied upon to distinguish the invention from the prior art. Until that time, the Examiner interprets this limitation as merely "groups."

5. Claims 4, 11, and 18 recite that a "file editing unit" is necessary to "[edit] said variation rule file by incorporating said actual configuration information," or a similar limitation. In contrast, claim 2 recites that "said delay information operating part modifies said design information on the basis of said variation, and said delay information file includes the modified design information." What specific feature of the "variation rule file" requires the generically described "file editing unit?" Does the disclosure contain any explanation as to why a "file editing unit" is necessary?

Claim 4 is also awkward when regarded as an independent claim, that is, incorporating all of the limitations of claim 1 from which it depends. If claim 1 represents a complete and functional system, the role of the "file editing unit" of claim 4 seems entirely inconsequential fo the system of claim 1. What purpose is served by "edit[ing] said variation rule file by incorporating said actual configuration information?" It is unclear how the components recited therein have any meaningful contribution to the system of claim 1.

6. As described in greater detail in the rejection under 35 U.S.C. § 112, second paragraph, the language of claim 5 appears defective. In addition, a step of "verifying" with no resulting action is an inconsequential step. Of course, anticipation is shown when the prior art discloses the claimed element or its equivalent (MPEP 2114, 2183, etc.) In this case, an inconsequential step of "verifying" would be anticipated by nearly any disclosure. It is unknown how Applicants would establish patentability with such a limitation.

Claims 12 and 19 apparently recite that variation in the power supply voltage in a chip is used to transmit a signal. This language is at least unconventional. If this is indeed Applicants' invention, clarification and specific citation of support in the disclosure is required.

7. Claims 6, 13, and 20 recite a similarly inconsequential step of calculating. The result of the recited calculation is not used by the system. The claimed limitations appear to accomplish nothing useful to the system and therefore would be anticipated by nearly any disclosure in the prior art.

8. Similarly to claim 3, claims 7, 14 and 21 recite "said delay information operating unit divides said information on wiring temperature into segments corresponding to said size of said group," or a similar limitation, which apparently requires dividing information into groups. Perhaps Applicants are referring to dividing the wire, not the information on wire temperature, into groups. It is unclear what is being referred to by "said size" and "said group," although presumably it is the size of the groups which result from dividing said information on wiring temperature into segments.

9. Claims 23, 25, and 27 recites an inconsequential step of calculating. Applicants' use of the term "capacity" is also unconventional and requires clarification.

While many of these objections fail to rise to the level of a rejection under 35 U.S.C. § 112, second paragraph, the language is generally so broad that Applicants may find it challenging to overcome any prior art rejections. The claim language generally lacks the specificity necessary for expedient prosecution.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 5 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites "verifying whether abnormality is caused in the transmission of a

signal variation in said power supply voltages in the same chip," the meaning of which is unknown. Although Applicants have cited support for this claim in the specification at (page 13, lines 5-31; page 14, lines 11-15; page 14, lines 15-20) it remains unclear how this claim language relates to or is supported by the specification. The limitations of claim 5 appear to require a step of transmitting a "signal variation" by means of power supply voltages, where a "signal variation" is apparently a range of values for a signal. This claim language appears to be disconnected from the rest of the claims and the disclosed invention. Perhaps this claim contains a typographical error or recites terminology that is ambiguously defined.

11. Claims 23, 25, and 27 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims recite "wherein said electrical and physical characteristics include capacity" which renders the claim vague and indefinite. What is meant "capacity" in the context of the invention? Applicants are respectfully requested to cite specific support from the disclosure which explains what is meant by the term "capacity" as used in these claims. It is similarly unknown what is meant by "variation of signal level caused by variation in capacities." These claims will be treated with claims 22, 24, and 26 respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-27 are rejected under 35 U.S.C. § 102(e) as being anticipated by US Patent No. 6,484,297 to Dixit et al. (Dixit).

Regarding claim 1, Dixit discloses a logical simulation system [*"The present invention generates the delay data points (Dnom) by conducting SPICE simulation on the cell* [...]" (column 5, lines 7-20)] comprising:

A delay information operating part that receives information regarding the electrical and physical characteristics which influence the operation of an integrated circuit, the functional equivalence of a "variation rule file" ["[...] *conducting a SPICE simulation on the cell by using the parameters for the nominal condition (i.e., nominal P* [process], *V* [voltage], *and T* [temperature]*) and the transistor level netlist of the cell. However, during the simulation, the input ramptime (R) and the output load (F) of the cell are varied within a respective range."* (column 5, lines 7-20) Dixit implicitly discloses the SPICE simulation component that receives both the nominal P, V, and T data as well as the varied R and F data.];

And receiving design information ["[...] *conducting a SPICE simulation on the cell by using the parameters for the nominal condition (i.e., nominal P* [process], *V* [voltage], *and T* [temperature]*) and the transistor level netlist of the cell.* (column 5, lines 7-20) Dixit implicitly discloses the SPICE simulation component that receives the "design information".];

Prepares delay information in consideration of each influence of said variation information regarding the electrical and physical characteristics which influence the operation of an integrated circuit on the basis of that variation information and the design information ["[...]

delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells. (column 4, line 66 – column 5, line 6); *"In step 140, after solving for Kp, Kt, and Kv, they are applied to the following equation to solve for any new delays for the cells* [...]" (column 7, lines 45-59)]; and

A logical simulation part which receives said design information and said delay information to carry out a logical simulation of the integrated circuit [*"The present invention provides for accurate calculation of delays for cells in ASICs."* (column 4, lines 32-45); The utility of a delay calculation in an integrated circuit cell is to accurately simulate the integrated circuit. Dixit discloses the use of a SPICE simulator that uses a delay calculation (column 5, lines 7-20). Dixit therefore implicitly discloses an improved delay calculation for use in a SPICE simulator.]

In response, Applicants' argue primarily that:

> However, *Dixit* does not teach a delay information operating part further receiving design information of an integrated circuit to prepare a delay information file incorporating each influence of variation of electrical and physical characteristics for each location in a chip on the basis of a variation rule file and design information, as required by claim 1.

The Examiner respectfully traverses this argument as follows.

The claim language "to prepare a delay information file incorporating each influence of said variation for each location in the chip on the basis of said variation rule file and design information" is clearly a statement of intended use in the context of a system claim which recites components such as a delay information operating part and a logical simulation part. As admitted by Applicants:

> In *Dixit*, delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells (Col. 4, line 66 – Col. 5, line 6). Further, *Dixit*

> discloses that given R and F, the values for Kp, Kt and Kv can be solved by using the discussed equations (Col. 7, lines 45-46). Further, after solving for Kp, Kt and Kv, those values are applied to another equation to solve for any new delays for the cells (Col. 7, lines 47-59).

Therefore Dixit discloses preparing a "delay information file" (the collection of calculated delays for the cells) incorporating the influence said variation for each location in the chip (each cell) based on said variation rule file (the collection of equations) and design information (P, V, T, R, and/or F). Of course, actually preparing this file is not required by the claim language.

Applicants' arguments for independent claim 8 and 15 refer to those arguments addressed above. Applicants' arguments for dependent claims 9-14, 16-21, and 22-27 refer to those arguments addressed above.

Applicants' arguments have been fully considered but have been found unpersuasive.

Claim 8 recites the method performed by the system of claim 1. Dixit teaches a computer-implemented method (column 7, line 60 – column 8, line 10) and is therefore rejected for the same reasons given above for claim 1.

Claim 15 recites a computer-readable recorded medium which causes a computer to execute the method of claim 1. Dixit teaches a computer-implemented method (column 7, line 60 – column 8, line 10) and is therefore rejected for the same reasons given above for claim 1.

Regarding claims 2, 9, and 16, Dixit discloses modifying said design information on the basis of said variation and said delay information file includes the modified design information

["[...] *propagation delays and the setup/hold time delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells* [...]" (column 4, lines 33-46); *"In step 115, the value for V is changed from Vnom to another voltage value within the operating range of the cell (e.g., 95% of Vnom or 105% of Vnom) while T and P remain at their nominal values A SPICE simulation is conducted with the new V value."* (column 6, lines 1-5)].

Regarding claims 3, 10, and 17, Dixit discloses classifying said information on variation into groups of an arbitrary size which constitute the chip and wherein said delay information file is prepared so that the influence of said variation is incorporated for every said group [*"The integrated circuit 26 further comprises a large number* [...] *of small cells 32. Each cell 32 represents a single logic element, such as a gate, or several logic elements interconnected in a standardized manner to perform a specific function."* (column 2, lines 28-35) *"It is an object of the present invention to provide methods for calculating delays for cells in an ASIC."* (column 4, lines 29-31)].

Regarding claims 4, 11, and 18, Dixit discloses that the design information includes actual configuration information which is information on the position of a cell of the integrated circuit in an actual configuration and a file editing unit which receives said variation rule file and edits said variation rule file by incorporating said actual configuration information [*"The output of partitioning is a set of blocks, along with the interconnections required between blocks. The set of interconnections required is the netlist."* (column 2, lines 59-67); *"The present invention*

generates the delay data points (Dnom) by conducting SPICE simulation on the cell by using the parameters for the nominal condition [...] *and the transistor level netlist of the cell."* (column 5, lines 7-20) As used by Dixit, "netlist" meets the broadest reasonable interpretation of "information on the position of a cell of the integrated circuit in an actual configuration". *"Thus, for a given R and F, the values for Kp, Kt and Kv can be solved by using the above equations."* (column 7, liens 45-46)]

Regarding claims 5, 12, and 19, the specific limitations required to anticipate these claims remains unknown. However, Dixit discloses that the method considers power supply voltage in the delay calculation [*"A new delay can be solved for any given new P, V, T, R and F by using the above equation."* (column 7, lines 45-59)].

Regarding claims 6, 13, and 20, Dixit discloses that the electrical and physical characteristics include a power supply voltage ["[...] *delays are computed by considering not only the* [...] *voltage*" (column 4, lines 33-46)] and the method calculates the effects of variation in the power supply voltage and a delay time of signal transmission caused by the variation of the signal level [*"A new delay can be solved for any given new P, V, T, R and F using the above equation."* (column 7, lines 45-59)].

Regarding claims 7, 14, and 21, Dixit discloses that design information includes wiring temperature ["[...] *conducting a SPICE simulation on the cell by using the parameters for the*

nominal condition (i.e., nominal P [process], *V* [voltage], *and T* [temperature]*) and the transistor level netlist of the cell.* (column 5, lines 7-20)];

The logical simulation method comprises dividing said information on wiring temperature into segments corresponding to the size of the group and the delay information is prepared so that the influence of said variation is considered for every segment; and said delay information file is prepared so that the influence of said variation is incorporated for every said segment [*"The output of partitioning is a set of blocks, along with the interconnections required between blocks. The set of interconnections required is the netlist."* (column 2, lines 59-67); *"The present invention generates the delay data points (Dnom) by conducting SPICE simulation on the cell by using the parameters for the nominal condition* [...] *and the transistor level netlist of the cell."* (column 5, lines 7-20)].

Regarding claims 22-27, Dixit discloses said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each location in the chip, and variation in junction temperature [*"*[...] *delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells.* (column 4, line 66 – column 5, line 6); *"In step 140, after solving for Kp, Kt, and Kv, they are applied to the following equation to solve for any new delays for the cells* [...]" (column 7, lines 45-59)].

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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3/15/06